AMENDMENT TO THE CLAIMS

1.(currently amended) A circuit, comprising:

a multiplexer having a select input and a sequence of analog outputs that are selected from a plurality of analog inputs provided by an analog system;

a reference source providing a first reference;

an analog-to-digital converter receiving the sequence of analog outputs and the first reference, and providing a sequence of digital outputs; and

a control circuit actuating the select input to select the sequence of the analog outputs, the control circuit comparing the sequence of digital outputs to a stored sequence of normal ranges that correspond with the digital outputs to provide an error output when at least one of the digital outputs is not in its normal range, the control circuit further providing a real time output that represents a useful parameter of the analog system.

2.(original) The circuit of Claim 1 wherein at least two of the normal ranges are non-overlapping.

3.(original) The circuit of Claim 2 wherein short-circuiting of two of the plurality of analog inputs causes at least one of the digital outputs to exceed its corresponding normal range.

4.(original) The circuit of Claim 2 wherein the select input comprises a digital word with a series of bits, and wherein a sticking of one of the series of bits causes at least one of the digital outputs to exceed its corresponding normal range.

5.(original) The circuit of Claim 2 wherein the sequence of digital outputs comprises digital words with a series of bits, and wherein a sticking of one of the bits causes at least one of the digital outputs to exceed its corresponding normal range.

6.(original) The circuit of Claim 1, wherein each normal range is different and does not overlap another normal range.

7.(original) The circuit of Claim 1, wherein:

the normal ranges comprise an odd range and an even range, and

the plurality of analog inputs are connected to the multiplexer in a numbered sequence such that odd-numbered analog inputs generate digital outputs that are in the odd range and even-numbered analog inputs generate digital outputs that are in the even range.

8.(original) The circuit of Claim 7, further comprising:

a first switch;

wherein the reference source generates a second reference that is different than the first reference; and

wherein the control circuit controls the first switch to couple the first reference to the analog-to-digital converter when an odd-numbered analog input is selected, and controls the first switch to couple the second reference to the analog-to-digital converter when an even-numbered analog input is selected.

9.(original) The circuit of Claim 8, further comprising:

a second switch; and

wherein the analog-to-digital converter comprises first and second differential inputs, the analog output is connected to the first differential input; and the

control circuit controls the second switch to connect a selected one of the second reference and a common conductor to the second differential input.

10.(original) The circuit of Claim 1 wherein the control circuit controls the reference source to generates the first reference at a first level when an odd-numbered analog input is selected, and to generate the first reference at a second level when an even-numbered analog input is selected.

11.(currently amended) A method of detecting an error, comprising:

providing a plurality of analog inputs generated by an analog system;

generating a sequence of analog outputs that are selected from ~~a~~ **the** plurality of analog inputs as a function of a select input;

providing a first reference;

receiving the sequence of analog outputs and the first reference, and providing a sequence of digital outputs that represent the sequence of analog outputs; and

actuating the select input to select the sequence of the analog outputs; ~~and~~

comparing the sequence of digital outputs to a stored sequence of normal ranges that correspond with the digital outputs to provide an error output when at least one of the digital outputs is not in its normal range; and

providing a real time output that represents a useful parameter of the analog system.

12.(original) The method of Claim 11 wherein at least two of the normal ranges do not overlap one another.

13.(original) The method of Claim 12 wherein at least one of the analog inputs exceeds its corresponding normal range when two of the plurality of analog inputs short circuit to one another.

14.(original) The method of Claim 12 wherein at least one of the digital outputs exceeds its corresponding normal range when one output bit in the select input sticks.

15.(original) The method of Claim 12 wherein at least one of the digital outputs exceeds its corresponding normal range when one output bit in the digital outputs sticks.

16.(original) The method of Claim 11, wherein each normal range differs from the other normal ranges and does not overlap another normal range.

17.(original) The method of Claim 11, further comprising:

providing the normal ranges as an odd range and an even range, and

connecting the plurality of analog inputs to a multiplexer in a numbered sequence such that odd-numbered analog inputs generate digital outputs that are in the odd range and even-numbered analog inputs generate digital outputs that are in the even range.

18.(original) The method of Claim 17, further comprising:

providing a first switch;

generating a second reference that is different than the first reference; and

controlling the first switch to couple the first reference to an analog-to-digital converter when an odd-numbered analog input is selected, and controlling the first

switch to couple the second reference to the analog-to-digital converter when an even-numbered analog input is selected.

19.(original) The method of Claim 18, further comprising:

providing a second switch;

providing first and second differential inputs on the analog-to-digital converter,

connecting the analog output to the first differential input; and

controlling the second switch to connect a selected one of the second reference and a common conductor to the second differential input.

20.(original) The method of Claim 11, further comprising:

controlling a reference source to generates the first reference at a first level when an odd-numbered analog input is selected, and

controlling the reference source to generate the first reference at a second level when an even-numbered analog input is selected.

21.(currently amended) A circuit, comprising:

a multiplexer having a select input and a sequence of analog outputs that are selected from a plurality of analog inputs provided by an analog system;

a reference source providing a first reference;

an analog-to-digital converter receiving the sequence of analog outputs and the first reference, and providing a sequence of digital outputs; ~~and~~

means for actuating the select input to select the sequence of the analog outputs, and for comparing the sequence of digital outputs to a stored sequence of normal

ranges that correspond with the digital outputs to provide an error output when at least one of the digital outputs is not in its normal range; and

means for providing a real time output that represents a useful parameter of the analog system.

22.(original) The circuit of Claim 21 wherein at least two of the normal ranges are non-overlapping.

23.(original) The circuit of Claim 22 wherein short-circuiting of two of the plurality of analog inputs causes at least one of the digital outputs to exceed its corresponding normal range.

24.(original) The circuit of Claim 22 wherein the select input comprises a digital word with a series of bits, and wherein a sticking of one of the bits causes at least one of the digital outputs to exceed its corresponding normal range.

25.(original) The circuit of Claim 22 wherein the sequence of digital outputs comprises digital words with a series of bits, and wherein a sticking of one of the bits causes at least one of the digital outputs to exceed its corresponding normal range.